REMARKS

This communication responds to the Office Action mailed on April 7, 2008.

Claims 1, 10, 15 and 17 are amended, claims 3-5 are canceled, and no claims are added in this communication. As a result, claims 1-2 and 6-21 are now pending in this Application.

Objections to the Drawings

The drawings were objected to under 37 CFR 1.83(a) as not showing every feature of the invention specified in the claims. The objection to the drawings was maintained over the arguments which Applicants provided in the Response filed March 10, 2008.

In response to the Applicant's arguments, the Office admitted that Figures 4A and 4B shows "Did transaction complete", "status bit remains set" and "reset status bit". However, the Office asserts that Figures 4A and 4B do not show the feature "retrying the first bus transaction and each subsequent non modifying bus transaction for the shared resource until the status bit is clear" as recited in claim 1. The Applicants respectfully disagree.

Referring to Figures 4A and 4B, it is noted that an arrow is shown in Figure 4A pointing to block 410 from block 414 and thus forming a loop, and that an arrow is shown in Figure 4B pointing to block 410 from block 416 and thus forming a loop 410 → 414 → 416 → 410. It thus can be seen that steps 410 and 414 of Figure 4A, as well as steps 410, 414 and 416 of Figure 4B actually show and support the feature "**retrying the first bus transaction and each subsequent non modifying bus transaction for the shared resource until the status bit is clear**" as recited in claim 1.

Applicants have amended claim 1 by replacing the term "the **second** bus transaction" with "the **nonmodifying** bus transaction", and thus believe that the feature "**wherein the status indicator is a status bit to indicate whether the nonmodifying bus transaction completes, if the nonmodifying bus transactions complete, the status bit is cleared, otherwise status bit remains as being set**" as recited in amended claim 10 is supported by, for example Figure 4B and page 8, lines 17-19 and 26-31 of the Specification.

Claims 3-6 recite ways to clear the status bit. Referring again to Figures 4A and 4B, "CLEAR STATUS BIT" is shown in step 412 of Figures 4A, as well as steps 412 and 418 of

Figure 4B. In specification, page 7, lines 13-18 and page 8, lines 26-31 describe instances in detail how to clear the status bit. Thus, it is believed that Figures 4A and 4B, which include multiple instances of element 412, already satisfies the requirements of 37 CFR § 1.83(a). Therefore, no amendment to the drawings should be necessary. The discussion for drawings with respect to claims 1 and 3-6 also apply to drawings with respect to claims 7-9.

Therefore, the Applicants respectfully submit that the drawings of the present Application meet the requirement of 37 CFR 1.83(a) and respectfully request reconsideration and withdrawal of the objection to the drawings.

§112 Rejection of the Claims

Claims 10-21 were rejected under 35 USC § 112, first paragraph, as failing to comply with the written description requirement. Applicants have amended claims 10, 15 and 17 by replacing the term "the **second** bus transaction" with "the **nonmodifying** bus transaction", and thus believes that the feature "**wherein the status indicator is a status bit to indicate whether the nonmodifying bus transaction completes, if the nonmodifying bus transactions complete, the status bit is cleared, otherwise status bit remains as being set, and the status bit is randomly reset**" as recited in amended claims 10, 15 and 17 is supported by, for example Figure 4B and page 8, lines 17-19 and 26-31 of the Specification.

Claims 10-21 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicants have amended claims 10, 15 and 17 by replacing the term "the **second** bus transaction" with "the **nonmodifying** bus transaction", which has sufficient antecedent basis, and thus believes that this amendment of claims 10, 15 and 17 overcomes the rejection of claims 10-21 under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

It is therefore respectfully requested that the rejection of claims 10-21 under 35 U.S.C. § 112 be reconsidered and withdrawn.

§103 Rejection of the Claims

Claims 1, 2, 4 and 5 were rejected under 35 USC § 103(a) as being unpatentable over Gillbert et al. (U.S. 6,041,376, hereinafter "Gillbert") in view of Arimilli et al. (U.S. 6,138,218, hereinafter "Arimilli").

Claims 3 and 6-20 were also rejected under 35 USC § 103(a) as being unpatentable over Gillbert in view of Arimilli and further in view of Donley et al. (U.S. 5,761,446, hereinafter "Donley").

Claim 21 was also rejected under 35 USC § 103(a) as being unpatentable over Gillbert in view of Arimilli further in view of Donley and further in view of Vogt et al. (U.S. 5,897,656, hereinafter "Vogt").

Applicants submit that none of the cited references (Gillbert, Arimilli, Donley and Vogt) discloses the feature "randomly resetting the status bit either as being set or as cleared" of amended claim 1.

Applicants agree with the Office Action's admission on page 23, 3rd paragraph, "Gillbert and Arimilli do not specifically show the use of randomly or pseudo-randomly." The Office Action then asserts, "Donley shows generating random number or Pseudo-random number (e.g., col. 3, lines 46-60)" and Donley "would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63." However, Donley does not show to randomly reset status bit either as being set or as cleared as claimed in claim 1. Referring to Donley, col. 3, lines 46-60, and col. 2, lines 61-63 as follows, with emphasis added:

> **The random number for such backoff / stretch delay** is preferably generated by a 9-bit pseudo-random number generator which provides a repeating 9-bit sequence every 511 clocks. Such a period (511 clock beats) should be long enough to prevent any retry pattern from developing on the bus--after which the 9-bit sequence will repeat. This random number generator is implemented as shown in FIG. 2 by Linear Feedback Shift Register SR, as fed by Control Register CR and suitable Combinational Logic stage CL. Register SR comprises nine (9) flip-flops (#0 thru #8) in series, and sharing input from Control bus 11 and the common clock CLK, plus a feedback from #4 and #0 via EX-NOR gate G. (col. 3, lines 46-60).

> Thus, an object hereof is to address "system livelock", especially with a "backoff" solution. A related object is to do so via "random backoff". Another related object to do so via a "stretch" mechanism, especially "**random stretch**". A further object is to implement such "random backoff" and/or "random stretch" mechanisms with addressing means which is adapted to generate the related random number (delay), especially where this is done with a linear feedback shift register, providing a "pseudo-random sequence". A related object is to do this also using control means adapted for selection of "window range" (width) and "offset" values used to generate a random backoff/random stretch count, programmed to provide a delay range which can resolve "livelock" and also enhance system performance. A further object is to address the problems here mentioned and to provide related features and advantages. (col. 2, lines 61-63).

It can be seen that the "random backoff" or "random stretch" mechanism of Donley, which is used to generate the related random number (delay), does not **randomly reset the status bit** as claimed in amended claim 1. Accordingly, the Office Action's above assertion does not justify the attempted conclusion that Donley discloses the feature "randomly resetting the status bit either as being set or as cleared" of claim 1.

Vogt does not remedy this defect of Gillbert, Arimilli and Donley. Thus, even combined, the cited references Gillbert, Arimilli, Donley and Vogt do not disclose the feature "randomly resetting the status bit either as being set or as cleared" of claim 1. For at least this reason, the Applicants submit that the cited references do not render amended claim 1 obvious.

This argument discussed with respect to amended claim 1 also applies to independent claims 7, 10, 15 and 17, which respectively have a similar feature to amended claim 1. Claims 2, 6, 8-9, 11-14, 16 and 17-21 are non-obvious as well, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03.

It is therefore respectfully requested that the rejection of claims 1-2 and 6-21 under 35 U.S.C. § 103 be reconsidered and withdrawn.

CONCLUSION

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney ((612) 373-6900) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 373-6900

By /Jun Wei/
Jun Wei
Reg. No. 55,717